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EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,030	SNYDER ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26* is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *18-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/10/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been presented for examination.

Priority

2. The Examiner acknowledges the Applicants claim to priority to U.S. Provisional Application Number 60/243,708 under 35 U.S.C. § 119(e).

Claim Objections

3. **Claim 1** is objected to because of the following informalities: The phrase on line 9 *"upon **an** time phrase"* should be re-written to *"upon a time phrase"*.

Appropriate correction is requested.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1-5 and 7, 8, 10-12, 13 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Circello et al. U.S. Patent 5,964,893** in view of **Bakker U.S. Patent 6,185,522.**

4.1 As regards independent **Claim 1** the *Cirello et al.* reference discloses, *A communication interface* **(Figure 2 item 30),** *for coupling a device under test (DUT)***(Figure 1 item 9** this is the device under test**),** *with an emulator device* **(Figure 1 item 10**, this is the emulator device**),** *the emulator device implementing the DUT and executing instructions in lock-step with the DUT* (Synchronization is the functional equivalent of "lock-step" **Col. 27 lines 23-39 and Col. 29 lines 65-67, Col. 30 lines 1-20),** *a time dependent data transport portion that communicates serialized data between the DUT and the emulator device* **(Figure 2 item 30, Col. 4 lines 31-41, Col. 16 lines 31-49, Col. 17 lines 4-20, Col. 30 lines 22-35),** and the Time dependent data transport portion transports varying types of information depending upon a time phase of operation of the DUT and the emulator device **(Col. 5 lines 8-14).**

However, the *Cirello et al.* reference does not expressly disclose a clock portion that supplies clock information to the DUT and the emulator device.

The *Bakker* reference discloses a clock portion that supplies clock information to the DUT and the emulator device **(Figure 2 items 52 & 54 and Figure 3).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the clock teachings of the *Bakker* reference because, there is a need in the microcontroller emulation art to

accommodate the higher speed clocks being used in today's digital technology and still synchronize with the data stream needed during emulation (*Bakker* **Col. 3 lines 10-32).**

4.2 As regards dependent **Claim 2** the *Cirello et al.* reference does not expressly disclose a *bi-directional* data line.

The *Bakker* reference discloses a plurality of data lines with at least one being bi-directional **(Figure 3).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the data line teachings of the *Bakker* reference because, there is a need in the microcontroller emulation art to accommodate the higher speed clocks being used in today's digital technology and still synchronize with the data stream needed during emulation (*Bakker* **Col. 3 lines 10-32).**

4.3 As regards dependent **Claim 3** the *Cirello et al.* reference discloses a first time dependent unidirectional data line which is the functional equivalent of a *clock line* **(Figure 2 item 30** "DSCLK" and **Col. 4 line 38),** however, it does not expressly disclose a second bi-directional time dependent data line.

The *Bakker* reference discloses a second bi-directional time dependent data line, **(Figure 3).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the data line teachings of the *Bakker* reference because, there is a need in the microcontroller emulation art to accommodate the higher speed clocks being used in today's digital technology and still synchronize with the data stream needed during emulation (*Bakker* **Col. 3 lines 10-32).**

4.4 As regards dependent **Claim 4** the *Cirello et al.* reference discloses an internal clock line for the DUT **(Figure 2 item 30** "DSCLK"**),** however it does not expressly disclose a system clock line.

The *Bakker* reference discloses a system clock line **(Figure 3** "XTAL1(in)"**).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the clock line teachings of the *Bakker* reference because, there is a need in the microcontroller emulation art to accommodate the higher speed clocks being used in today's digital technology and still synchronize with the data stream needed during emulation **(***Bakker* **Col. 3 lines 10-32).**

4.5 As regards independent **Claim 5** the *Cirello et al.* reference discloses a communications interface **(Figure 2 item 30),** an emulator mode of operation *which describes the functional equivalent of an emulation device* **(Col. 10 lines 6-34),** executing instructions lock-step, *which is the functional equivalent of synchronization,* with the emulator device **(Col. 27 lines 23-39 and Col. 29 lines 65-67, Col. 30 lines 1-20),** where the interface comprises, a data line **(Figure 2 item 30, Col. 4 lines 31-41, Col. 16 lines 31-49, Col. 17 lines 4-20, Col. 30 lines 22-35),** and a clock line **(Figure 2 item 30** "DSCLK"**).**

However, the *Cirello et al.* reference does not expressly disclose implementing a microcontroller as an emulation device and a bi-directional data line and a second clock line.

The *Bakker* reference discloses implementing a microcontroller as an emulation device **(Figures 1 & 2),** a bi-directional data line **(Figure 3),** and a second clock line **(Figure 3** "XTAL1(in)"**).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the clock line teachings of the *Bakker* reference because, there is a need in the microcontroller emulation art to accommodate the higher speed clocks being used in today's digital technology and still synchronize with the data stream needed during emulation **(***Bakker* **Col. 3 lines 10-32).**

4.6 As regards dependent **Claim 7** the *Cirello et al.* reference discloses conveying interrupt data **(Col. 8 lines 32-48).**

4.7 As regards dependent **Claim 8** the *Cirello et al.* reference discloses break signals **(Col. 5 Lines 39-49).**

4.8 As regards dependent **Claim 10** the *Cirello et al.* reference discloses read/write commands during a halt **(Col. 9 lines 41-67 Col. 10 lines 1-12).**

4.9 As regards dependent **Claim 11** the *Cirello et al.* reference discloses conveying register information when in halt mode **(Col. 9 lines 40-55).**

4.10 As regards dependent **Claims 12 and 16** the *Cirello et al.* reference does not expressly disclose watchdog timer information.

The *Bakker* reference discloses watchdog timer information **(Col. 4 Lines 24-27).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the clock line teachings of the *Bakker* reference because, there is a need in the microcontroller emulation

art to accommodate the higher speed clocks being used in today's digital technology and still synchronize with the data stream needed during emulation **(*Bakker* Col. 3 lines 10-32).**

4.11 As regards dependent **Claim 15** the *Cirello et al.* reference does not expressly disclose the I/O data that is sent over the interface is sent fast enough to stay in sync with the execution of the next instruction.

The *Bakker* reference discloses the I/O data that is sent over the interface is sent fast enough to stay in sync with the execution of the next instruction **(Figure 3, Col. 4 lines 49-53).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the clock line teachings of the *Bakker* reference because, there is a need in the microcontroller emulation art to accommodate the higher speed clocks being used in today's digital technology and still synchronize with the data stream needed during emulation **(*Bakker* Col. 3 lines 10-32).**

5. Dependent **Claims 9 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Circello et al. U.S. Patent 5,964,893** in view of **Bakker U.S. Patent 6,185,522** and in further view of **Buckmaster et al. U.S. Patent 6,298,320** and **OFFICIAL NOTICE.**

5.1 As regards independent **Claim 5** please see paragraph **4.5** in this Office Action.

5.2 As regards dependent **Claim 9** the *Cirello et al.* reference does not expressly disclose using CAT5 cable.

"OFFICIAL NOTICE" The *Buckmaster* reference discloses a Network Interface **(Figure 2 Items 66 & 68),** and it is well known in the art that CAT5 cables are used with network interfaces.

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have used the teachings in the *Buckmaster* reference with the teachings in the *Cirello et al.* reference because, of the advantages of being able to start the software development process before the target embedded hardware is available (*Buckmaster* **Col. 2 lines 65-67 Col. 3 lines 1-3),** and also the use of networking facilitates the development of software over a network instead of the developer having to program EEPROMS or flash in order to test a new build of software.

5.3 As regards dependent **Claim 13** the *Cirello et al.* reference does not expressly disclose flash memory.

The *Buckmaster* reference discloses flash memory **(Figure 2 item 48).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have combined the teachings of the *Cirello et al.* reference with the teachings of the *Buckmaster* reference because, of the advantages of being able to start the software development process before the target embedded hardware is available (*Buckmaster* **Col. 2 lines 65-67 Col. 3 lines 1-3).**

6. Dependent **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Circello et al. U.S. Patent 5,964,893** in view of **Bakker U.S. Patent 6,185,522** and in further view of **Coehlo et al. U.S. Patent 6,223,272.**

6.1 As regards independent **Claim 5** please see paragraph **4.5** of this Office Action.

6.2 As regards dependent **Claim 6** the *Cirello et al.* reference does not expressly disclose the use of an FPGA for emulation.

The *Coehlo et al.* reference discloses the use of an FPGA for emulation **(Col. 4 Lines 15-25).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the teachings of the *Cirello et al.* reference with the teachings of the *Coehlo et al.* reference because, there is a need in the art to speed up testing of ASIC designs (*Coehlo et al.* **Col. 2 Lines 23-25).**

7. Dependent **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Circello et al. U.S. Patent 5,964,893** in view of **Bakker U.S. Patent 6,185,522** and in further view of **Young et al. U.S. Patent 6,107,826.**

7.1 As regards independent **Claim 5** please see paragraph **4.5** above.

7.2 As regards dependent **Claim 14** the *Circello et al.* reference does not expressly disclose using a programmable clock.

The *Young et al.* reference discloses the use of the functional equivalent of a programmable clock *a DLL or Delay Lock Look* **(Figure 1 item 102, Col. 1 Lines 22-45).**

It would have been obvious, to one of ordinary skill in the emulation art, to have used the DLL methods disclosed in the *Circello et al.* reference in combination with the emulation methods of the *Bakker* reference because, of the flexible and efficient manner in which clock signals can be routed through out an FPGA (*Young et al.* **Col. 2 Lines 22-30).**

8. Independent **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Swoboda et al. U.S. Patent 5,805,792** in view of **Belhaj U.S. Patent 6,564,179** and in further view of **"ICEBERG: An Embedded In-circuit Emulator Synthesizer for Microcontrollers" by Ing-Jer Huang and Tai-An Lu** here after referred to as the *Huang et al.* reference.

8.1 As regards independent **Claim 17** the *Swoboda et al.* reference discloses a 4-wire interface for use in an emulation system **(Figure 81 items 2111 Col. 50 lines 18-35),** a first interface line carrying the functional equivalent of a system clock and a second interface line for carrying the functional equivalent to an internal CPU clock **(Col. 48 lines 52-67, Col. 49 lines 1-9).**

However, the *Swoboda et al.* reference does not expressly disclose a *vitual microcontroller* and an ICE for microcontroller emulation.

The *Belhaj* reference discloses a *virtual microcontroller* **(Figure 1 item 102 and Col. 4 lines 5-12).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have combined the *emulation interface* methods of the *Swoboda et al.* reference with the *virtual micrcontroller* methods of the *Belhaj* reference because, the methods in the *Belhaj* reference provide for a more efficient method for programmers to develop software code **(Col. 2 lines 16-22).**

The *Huang et al.* reference discloses an In-Circuit Emulator for a microcontroller **(pages 590-585).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have combined the *emulation methods* of the *Swoboda et al.* reference with the *ICE* methods of the *Swoboda et al.* reference because, of the debugging support an ICE provides to a system developer (*Huang et al.* **Introduction page 580).**

Allowable Subject Matter

9. **Claim 26** is allowed.

9.1 **Claims 18-25** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Claims 1-26 have been presented for Examination. Claims 1-17 have been rejected. Claims 18-25 are objected to. Claim 26 is allowable. This Office Action is **Non-Final.**

10.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (571)272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC